IN THE CLAIMS:

Kindly amend the claims, as follows:

88. (Currently Amended) A semiconductor integrated circuit device, wherein the semiconductor integrated circuit device includes a substrate and a plurality of memory cells, and wherein each of the plurality of memory cell comprises:

a transistor,

wherein the transistor includes a gate;

a gate oxide,

wherein the gate oxide is arranged between the gate and the substrate;

a cell plate,

wherein the cell plate is separated from the gate by a predetermined distance, and

wherein a portion of the cell plate overlaps a portion of the gate; and

a dielectric material arranged between the cell plate, the gate and the substrate,

wherein the dielectric material comprises a high dielectric constant.

89. (Previously Presented) The semiconductor integrated circuit device of claim 88, wherein the gate comprises polysilicon.

90. (Previously Presented) The semiconductor integrated circuit device of claim 88, wherein the cell plate comprises one of polysilicon and a metal conductor.

91. (Canceled)

92. (Currently Amended) The semiconductor integrated circuit device of claim ~~91~~ 88, wherein the dielectric material comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

93. (Previously Presented) The semiconductor integrated circuit device of claim 88, wherein the cell plate and the gate are positioned in different planes.

94. (Previously Presented) The semiconductor integrated circuit device of claim 88, wherein the gate is substantially coplanar with another portion of the cell plate.

95. (Previously Presented) The semiconductor integrated circuit device of claim 88, wherein the semiconductor integrated circuit device is manufactured using a logic process.

96. (Previously Presented) The semiconductor integrated circuit device of claim 88, wherein the semiconductor integrated circuit device is manufactured using a DRAM process.

97. (Currently Amended) An apparatus for reducing area in a dynamic random access memory (DRAM) device, wherein the DRAM device includes a substrate means and a plurality of means for storing data, and wherein each of the plurality of means for storing data comprises:

a transistor means for switching,

wherein the transistor means includes a gate means;

a gate insulating means for insulating the gate means from the substrate means;

a cell plate means for providing an electric field,

wherein the cell plate means is separated from the gate means by a predetermined distance, and

wherein a portion of the cell plate means overlaps a portion of the gate means; and

a dielectric means for separating the cell plate means from the gate means and the substrate means,

wherein the dielectric means comprises a high dielectric constant.

98. (Previously Presented) The apparatus of claim 97, wherein the gate means comprises polysilicon.

99. (Previously Presented) The apparatus of claim 97, wherein the cell plate means comprises one of polysilicon and a metal conductor.

100. (Canceled)

101. (Currently Amended) The apparatus of claim ~~100~~ 97, wherein the dielectric means comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

102. (Previously Presented) The apparatus of claim 97, wherein the cell plate means and the gate means are positioned in different planes.

103. (Previously Presented) The apparatus of claim 97, wherein the gate means is substantially coplanar with another portion of the cell plate means.

104. (Previously Presented) The apparatus of claim 97, wherein the DRAM device is manufactured using a logic process.

105. (Previously Presented) The apparatus of claim 97, wherein the DRAM device is manufactured using a DRAM process.

106. (Currently Amended) A method of reducing area in a dynamic random access memory (DRAM) device, wherein the DRAM device includes a substrate and a plurality of memory cells, wherein each of the plurality of memory cells includes a transistor, wherein the transistor includes a gate and a cell plate, and wherein the method comprises the steps of:

arranging a gate oxide between the gate and the substrate;

separating the cell plate from the gate by a predetermined distance,

wherein a portion of the cell plate overlaps a portion of the gate; and

arranging a dielectric material between the cell plate, the gate and the substrate, wherein the dielectric material comprises a high dielectric constant.

107. (Previously Presented) The method of claim 106, wherein the gate comprises polysilicon.

108. (Previously Presented) The method of claim 106, wherein the cell plate comprises one of polysilicon and a metal conductor.

109. (Canceled)

110. (Currently Amended) The method of claim ~~109~~ 106, wherein the dielectric material comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

111. (Previously Presented) The method of claim 106, further comprising the step of:

positioning the cell plate and the gate in different planes.

112. (Previously Presented) The apparatus of claim 106, further comprising the step of:

positioning the gate substantially coplanar with another portion of the cell plate.

113. (Previously Presented) The method of claim 106, wherein the DRAM device is manufactured using a logic process.

114. (Previously Presented) The method of claim 106, wherein the DRAM device is manufactured using a DRAM process.

115. (Currently Amended) A semiconductor integrated circuit device, wherein the semiconductor integrated circuit device includes a substrate and a plurality of memory cells, and wherein each of the plurality of memory cell comprises:

a transistor,

wherein the transistor includes a gate;

a gate oxide,

wherein the gate oxide is arranged between the gate and the substrate;

a cell plate,

wherein the cell plate is laterally separated from the gate by a predetermined distance; and

a dielectric material arranged between the cell plate and the gate and between the cell plate and the substrate,

wherein the dielectric material comprises a high dielectric constant.

116. (Previously Presented) The semiconductor integrated circuit device of claim 115, wherein the gate comprises polysilicon.

117. (Previously Presented) The semiconductor integrated circuit device of claim 115, wherein the cell plate comprises one of polysilicon and a metal conductor.

118. (Canceled)

119. (Currently Amended) The semiconductor integrated circuit device of claim ~~118~~ 115, wherein the dielectric material comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

120. (Previously Presented) The semiconductor integrated circuit device of claim 115, wherein the semiconductor integrated circuit device is manufactured using a logic process.

121. (Previously Presented) The semiconductor integrated circuit device of claim 115, wherein the semiconductor integrated circuit device is manufactured using a DRAM process.

122. (Currently Amended) An apparatus for reducing area in a dynamic random access memory (DRAM) device, wherein the DRAM device includes a substrate means and a plurality of means for storing data, and wherein each of the plurality of means for storing data comprises:

a transistor means for switching,

wherein the transistor means includes a gate means;

a gate insulating means for insulating the gate means from the substrate means;

a cell plate means for providing an electric field,

wherein the cell plate means is laterally separated from the gate means by a predetermined distance; and

a dielectric means for separating the cell plate means from the gate means and the cell plate means from the substrate means,

wherein the dielectric means comprises a high dielectric constant.

123. (Previously Presented) The apparatus of claim 122, wherein the gate means comprises polysilicon.

124. (Previously Presented) The apparatus of claim 122, wherein the cell plate means comprises one of polysilicon and a metal conductor.

125. (Canceled)

126. (Currently Amended) The apparatus of claim ~~125~~ 122, wherein the dielectric means comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

127. (Previously Presented) The apparatus of claim 122, wherein the DRAM device is manufactured using a logic process.

128. (Previously Presented) The apparatus of claim 122, wherein the DRAM device is manufactured using a DRAM process.

129. (Currently Amended) A method of reducing area in a dynamic random access memory (DRAM) device, wherein the DRAM device includes a substrate and a plurality of memory cells, wherein each of the plurality of memory cells includes a transistor, wherein the transistor includes a gate and a cell plate, and wherein the method comprises the steps of:

arranging a gate oxide between the gate and the substrate;

laterally separating the cell plate from the gate by a predetermined distance; and

arranging a dielectric material between the cell plate and the gate and between the cell plate and the substrate,

wherein the dielectric material comprises a high dielectric constant.

130. (Previously Presented) The method of claim 129, wherein the gate comprises polysilicon.

131. (Previously Presented) The method of claim 129, wherein the cell plate comprises one of polysilicon and a metal conductor.

132. (Canceled)

133. (Currently Amended) The method of claim ~~132~~ 129, wherein the dielectric material comprises one of tantalum oxide, aluminum oxide, silicon nitride and oxinitride.

134. (Previously Presented) The method of claim 129, wherein the DRAM device is manufactured using a logic process.

135. (Previously Presented) The method of claim 129, wherein the DRAM device is manufactured using a DRAM process.

136. - 198. (Canceled)